IC Physical Verification in the Nanometer Era

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Abstract:

With the advancement in nanometer Integrated circuit (IC) design, the number of integrated devices over an IC has increased tremendously making the verification of an IC before fabrication a complex task. The talk will explore the critical role of Physical Verification in today's IC design landscape. We will discuss how shrinking geometries and increasing design complexity demand more rigorous and sophisticated verification techniques and we will present tools and flows that are needed to verify those IC chips before producing the final mask that will go into manufacturing to ensure high yield for those integrated circuit designs.

Bio:

Sherif Hammouda received his B.Sc and M.Sc degree in Electronics Engineering from Ain Shams university in Cairo, Egypt in 1996 and 2001 respectively. He earned his PhD in Electrical and Computer Engineering from the University of Calgary in Alberta, Canada in 2006. He joined Mentor Graphics Corporation in 1997 focusing on various areas in the EDA field covering Digital simulation, Analog & Mixed signal verification and IC Design and manufacturing physical verification. He is currently an Engineering Director in Siemens EDA, driving R&D activities for Calibre tools suite for IC Physical verification. His research interests cover Analog IC Design automation as well EDA solutions for Physical verification.